NEW SCHEME

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Third Semester B.E. Degree Examination, July/August 2004

Common to BM/EC/EE/TE/ML/IT/CS/IS

Logic Design

Time: 3 hrs. [Max.Marks : 100

Note: *Answer any FIVE full questions.*

1. (a) State the principle of duality with an examples. (4 Marks)

   (b) Prove the following using Boolean theorems.

   i) $(x + \overline{x}\,\overline{y})(\overline{x} + \overline{y}) + yz = \overline{y} + z$

   ii) $\overline{w}\,\overline{y}\,\overline{z} + wz + \overline{y}z + xyz = \overline{w}\,\overline{y} + wz + xz$ (8 Marks)

   (c) Transform each of the following canonical expressions into its other canonical form in decimal notation.

   i) $f(x,y,z) = \Sigma m(1,3,5)$

   ii) $f(w,x,y,z) = \pi M(0,2,5,6,7,8,9,11,12)$ (8 Marks)

2. (a) What are universal gates? Realize the basic gates using them. (4 Marks)

   (b) Using graphical procedure, obtain a NOR - gate realization of the Boolean expression

   $$f(a,b,c,d) = \overline{a}d + a\overline{d}(B + \overline{C})$$

   Also explain the steps to be followed in the said procedure. (8 Marks)

   (c) Using K-map, determine the minimal sum of product expression and realize the simplified expression using only NAND gates.

   $$f(w,x,y,z) = \pi M(0,2,3,7,8,9,10)$$ (8 Marks)

3. (a) Using Quenie - McCluskey method and prime implicant reduction, determine the minimal SOP expression for the following using decimal notations.

   $$f(w,x,y,z) = \pi M(0,4,5,9) \bullet d(1,7,13)$$ (10 Marks)

   (b) Explain the procedure for loading a K-Map using Map entered variable technique with an example. (6 Marks)

   (c) For the following single variable entered map, obtain the minimal product of sum expression (4 Marks)

W\xy	00	01	11	10
0	Z	0	Z	1
1	Z	$\overline{Z}$	1	0

Fig. Q. No. 3(c)

Contd.... 2

4. (a) Explain a 2-input NAND gate TTL with Totem-pole output with a neat circuit diagram. (7 Marks)

   (b) What do you mean by FET? Describe the operation of a n-channel enhancement type MOSFET with neat diagrams. Write the circuit symbol for the same. (9 Marks)

   (c) Write the circuit diagram of a two input CMOS NAND gate. (4 Marks)

5. (a) Design a single decade BCD adder and explain the design methodology in detail. (8 Marks)

   (b) Implement a full subtracter using a decoder and two NAND gates. (6 Marks)

   (c) What is a comparator? Briefly explain the organisation of a 1-bit comparator. (6 Marks)

6. (a) Implement the following Boolean function using 8:1 multiplexer.

   $$f(w,x,y,z) = \Sigma_m(0,1,5,6,8,10,12,15)$$ (6 Marks)

   (b) Using PROM realize the following expressions

   $$f_1 = \Sigma_m(0,1,3,5,7)$$
   $$f_2 = \Sigma_m(1,2,5,6)$$ (6 Marks)

   (c) Illustrate the use of PLA for combinational logic design with an example. (8 Marks)

7. (a) Design a mod-5 synchronous binary counter using clocked J-K flip-flops. (10 Marks)

   (b) Discuss how excitation tables, state tables and state diagrams are used to analyse a synchronous sequential network. (10 Marks)

8. Write short notes on :

   i) Incompletely specified functions

   ii) Irredundant conjunctive expressions

   iii) Network terminal behaviour

   iv) Race around condition.

(4×5=20 Marks)